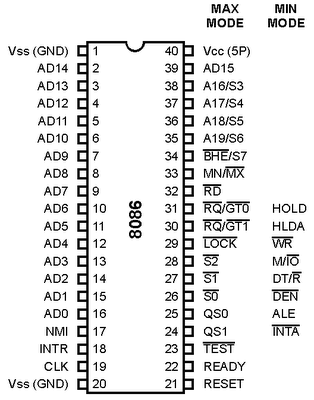
**Pin Diagram of 8086**



**QS1 and QS0**

These are queue status signals and are available at pin 24 and 25. These signals provide the status of instruction queue. Their conditions are shown in the following table −

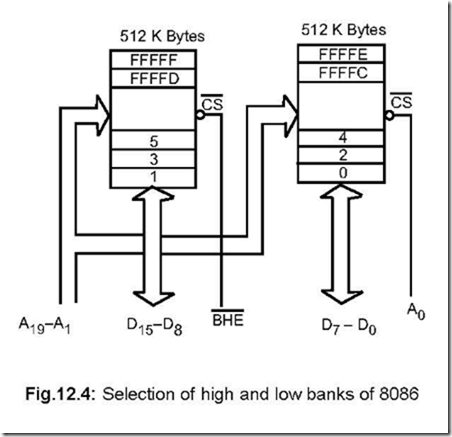
|  |  |  |
| --- | --- | --- |
| **QS0** | **QS1** | **Status** |
| 0 | 0 | No operation |
| 0 | 1 | First byte of opcode from the queue |
| 1 | 0 | Empty the queue |
| 1 | 1 | Subsequent byte from the queue |

**S0, S1, S2**

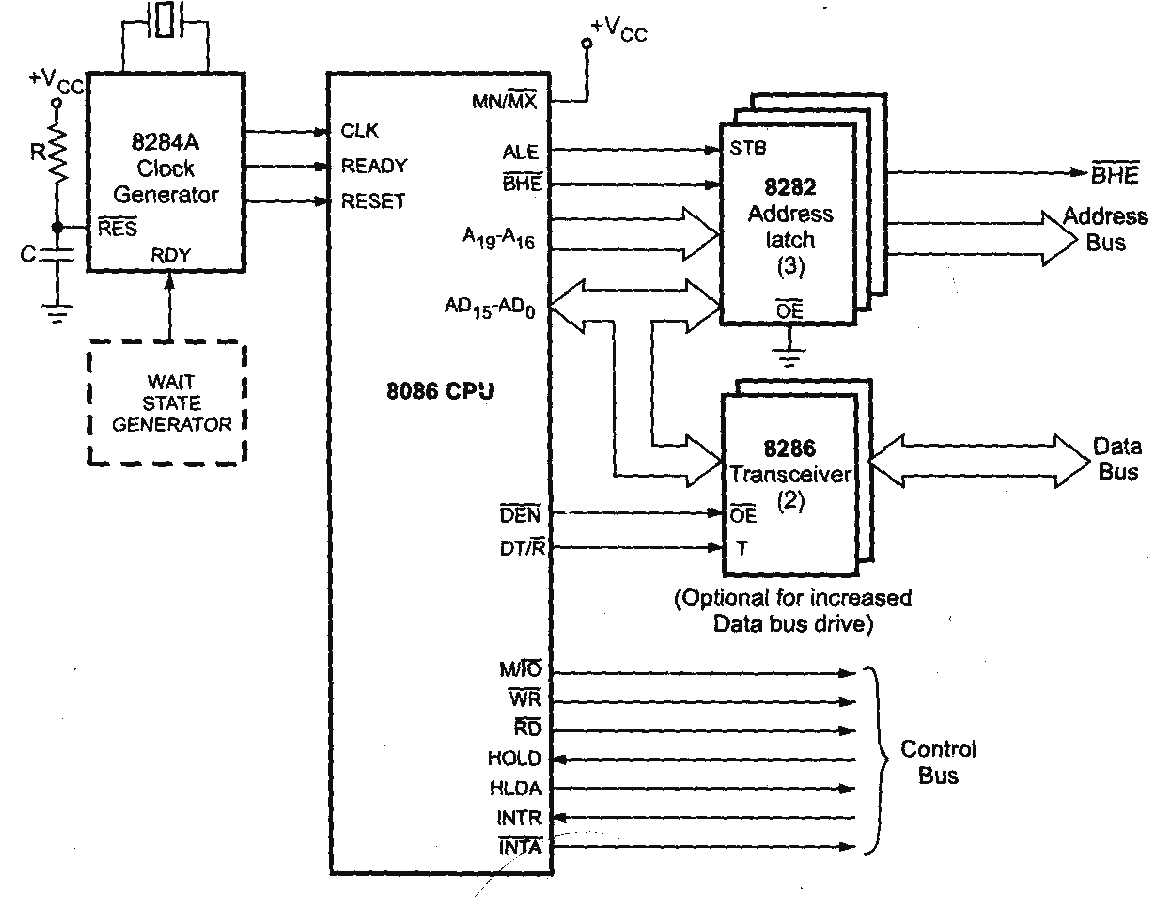
These are the status signals that provide the status of operation, which is used by the Bus Controller 8288 to generate memory & I/O control signals.

|  |  |  |  |
| --- | --- | --- | --- |
| **S2** | **S1** | **S0** | **Status** |
| 0 | 0 | 0 | Interrupt acknowledgement |
| 0 | 0 | 1 | I/O Read |
| 0 | 1 | 0 | I/O Write |
| 0 | 1 | 1 | Halt |
| 1 | 0 | 0 | Opcode fetch |
| 1 | 0 | 1 | Memory read |
| 1 | 1 | 0 | Memory write |
| 1 | 1 | 1 | Passive |

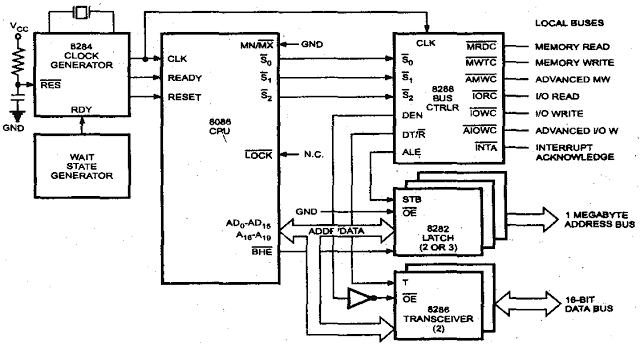
**8086 Memory Organisation (Even/odd Memory Banks in 8086**)

[](http://www.google.co.in/url?sa=i&rct=j&q=&esrc=s&source=images&cd=&cad=rja&uact=8&ved=0ahUKEwjMiuS6o_nVAhVFOo8KHUXgCPMQjRwIBw&url=http://8051-microcontrollers.blogspot.com/2014/10/memory-organisation.html&psig=AFQjCNGM-BjFMOSPsDY3PCwgIE_z1C5JaA&ust=1503987243376606)

**8086 System in Minimum Mode**

[](https://www.google.co.in/url?sa=i&rct=j&q=&esrc=s&source=images&cd=&cad=rja&uact=8&ved=0ahUKEwj_rcLMpvnVAhVHtY8KHdjaC6AQjRwIBw&url=https://mediatoget.blogspot.com/2012/09/&psig=AFQjCNEQ7CNJqPV-I9I7kCWebPRyciPW1w&ust=1503988004751884)

**8086 System in Maximum Mode**

[](https://www.google.co.in/url?sa=i&rct=j&q=&esrc=s&source=images&cd=&cad=rja&uact=8&ved=0ahUKEwiKx7LxpvnVAhUKo48KHd-AAIoQjRwIBw&url=https://mediatoget.blogspot.com/2012/&psig=AFQjCNEQ7CNJqPV-I9I7kCWebPRyciPW1w&ust=1503988004751884)

|  |  |  |  |
| --- | --- | --- | --- |
|  |  |  |  |